CLAIMS

What is claimed is:

1. A method comprising:
searching an associative memory cache using a search key;
in response to a miss at the associative memory cache, accessing a primary associative memory;
identifying in the primary associative memory an entry matching the search key and a number of overlapping entries; and
creating a non-overlapping entry, the non-overlapping entry having a range that includes at least a portion of a range of the matching entry and that does not include ranges of the overlapping entries.

2. The method of claim 1, wherein the matching entry comprises a highest priority matching entry.

3. The method of claim 1, wherein the range of the non-overlapping entry includes the largest possible portion of the range of the matching entry.

4. The method of claim 1, further comprising entering the non-overlapping entry into the associative memory cache.

5. The method of claim 4, further comprising:
identifying an existing entry in the associative memory cache for replacement; and
replacing the identified existing entry with the non-overlapping entry.

6. The method of claim 1, wherein creating the non-overlapping entry comprises:
determining a comparand for the non-overlapping entry; and
using a priority of the matching entry as a priority of the non-overlapping entry.

7. The method of claim 6, wherein creating the non-overlapping entry further comprises using data associated with the matching entry as data associated with the non-overlapping entry.

8. The method of claim 6, wherein determining the comparand for the non-overlapping entry comprises determining a binary range.

9. The method of claim 8, wherein the associative memory cache comprises a ternary content addressable memory (CAM).

10. The method of claim 6, wherein determining the comparand for the non-overlapping entry comprises determining a non-binary range.

11. The method of claim 10, wherein the associative memory cache comprises a boundary addressable memory (BAM).

12. The method of claim 6, wherein determining the comparand for the non-overlapping entry comprises using the search key as the comparand.

13. The method of claim 12, wherein the associative memory cache comprises a binary CAM.

14. An apparatus comprising:

an associative memory cache;

a primary associative memory;

a cache control coupled with each of the associative memory cache and the primary associative memory, the cache control to search the associative memory cache using a search key and, in response to a miss, access the primary associative memory to identify an entry matching the search key and a number of overlapping entries; and

a conversion module coupled with the cache control, the conversion module to create a non-overlapping entry, the non-overlapping entry having a range that includes at least a portion of a range of the matching entry and that does not include ranges of the overlapping entries.

15. The apparatus of claim 14, wherein the matching entry identified by the cache control comprises a highest priority matching entry.

16. The apparatus of claim 14, further comprising a search client coupled with the cache control, the search client to issue a search request to the cache control, the search request including the search key.

17. The apparatus of claim 14, further comprising replacement logic coupled with the cache control, the replacement logic to select an existing entry in the associative memory cache for replacement by the non-overlapping entry.

18. The apparatus of claim 14, wherein to create the non-overlapping entry, the conversion module determines a comparand for the non-overlapping entry and uses a priority of the matching entry as a priority of the non-overlapping entry.

19. The apparatus of claim 18, wherein to create the non-overlapping entry, the conversion module uses data associated with the matching entry as data associated with the non-overlapping entry.

20. The apparatus of claim 18, wherein the comparand comprises one of a binary range and a non-binary range.

21. The apparatus of claim 14, further comprising a second associative memory cache coupled with the cache control.

22. The apparatus of claim 14, wherein the associative memory cache, the primary associative memory, the cache control, and the conversion module are located on a single integrated circuit device.

23. The apparatus of claim 14, wherein the associative memory cache comprises an off-chip associative memory.

24. The apparatus of claim 14, wherein the primary associative memory comprises an off-chip associative memory.

25. The apparatus of claim 14, wherein the associative memory cache comprises one of a binary content addressable memory (CAM), a ternary CAM, and a boundary addressable memory (BAM).

26. The apparatus of claim 14, wherein the primary associative memory comprises one of a ternary CAM and a BAM.

27. The apparatus of claim 14, wherein the primary associative memory comprises:
a memory; and
a search engine coupled with the memory and the cache control, the search engine including an algorithm to utilize the memory as an associative memory.

28. The apparatus of claim 27, wherein the memory comprises one of a static random access memory (SRAM) and a dynamic random access memory (DRAM).

29. The apparatus of claim 27, wherein the memory comprises an off-chip memory.

30. A network processor comprising:
an associative memory cache;
a search engine coupled with a dynamic random access memory (DRAM), the search engine including an algorithm to utilize the DRAM as an associative memory;
a cache control coupled with each of the associative memory cache and the search engine, the cache control to search the associative memory cache using a search key and, in response to a miss, access the DRAM to identify an entry matching the search key and a number of overlapping entries; and
a conversion module coupled with the cache control, the conversion module to create a non-overlapping entry, the non-overlapping entry having a range that includes at least a portion of a range of the matching entry and that does not include ranges of the overlapping entries.

31. The network processor of claim 30, wherein the matching entry identified by the cache control comprises a highest priority matching entry.

32. The network processor of claim 30, further comprising a search client coupled with the cache control, the search client to issue a search request to the cache control, the search request including the search key.

33. The network processor of claim 30, wherein the search key is received from an off-chip search client.

34. The network processor of claim 30, further comprising replacement logic coupled with the cache control, the replacement logic to select an existing entry in the associative memory cache for replacement by the non-overlapping entry.

35. The network processor of claim 30, wherein to create the non-overlapping entry, the conversion module determines a comparand for the non-overlapping entry and uses a priority of the highest priority matching entry as a priority of the non-overlapping entry.

36. The network processor of claim 35, wherein to create the non-overlapping entry, the conversion module uses data associated with the highest priority matching entry as data associated with the non-overlapping entry.

37. The network processor of claim 35, wherein the comparand comprises one of a binary range and a non-binary range.

38. The network processor of claim 30, further comprising a second associative memory cache coupled with the cache control.

39. The network processor of claim 38, wherein the second associative memory cache comprises an off-chip associative memory.

40. The network processor of claim 30, wherein the associative memory cache comprises one of a binary content addressable memory (CAM), a ternary CAM, and a boundary addressable memory (BAM).

41. The network processor of claim 30, wherein the DRAM comprises part of the network processor.

42. An article of manufacture comprising:
a machine accessible medium providing content that, when accessed by a machine, causes the machine to
search an associative memory cache using a search key;
in response to a miss at the associative memory cache, access a primary associative memory;
identify in the primary associative memory an entry matching the search key and a number of overlapping entries; and
create a non-overlapping entry, the non-overlapping entry having a range that includes at least a portion of a range of the matching entry and that does not include ranges of the overlapping entries.

43. The article of manufacture of claim 42, wherein the matching entry comprises a highest priority matching entry.

44. The article of manufacture of claim 42, wherein the range of the non-overlapping entry includes the largest possible portion of the range of the matching entry.

45. The article of manufacture of claim 42, wherein the content, when accessed, further causes the machine to enter the non-overlapping entry into the associative memory cache.

46. The article of manufacture of claim 45, wherein the content, when accessed, further causes the machine to:
identify an existing entry in the associative memory cache for replacement; and
replace the identified existing entry with the non-overlapping entry.

47. The article of manufacture of claim 42, wherein the content, when accessed, further causes the machine, when creating the non-overlapping entry, to:
determine a comparand for the non-overlapping entry; and
use a priority of the matching entry as a priority of the non-overlapping entry.

48. The article of manufacture of claim 47, wherein the content, when accessed, further causes the machine, when creating the non-overlapping entry, to use data associated with the matching entry as data associated with the non-overlapping entry.

49. The article of manufacture of claim 47, wherein the comparand comprises one of a binary range and a non-binary range.